MANUAL OF OPERATION

FOR

MODEL 1320 TEST SET

INTERNATIONAL
DATA
SCIENCES INC.
LINCOLN, R.I., U.S.A.

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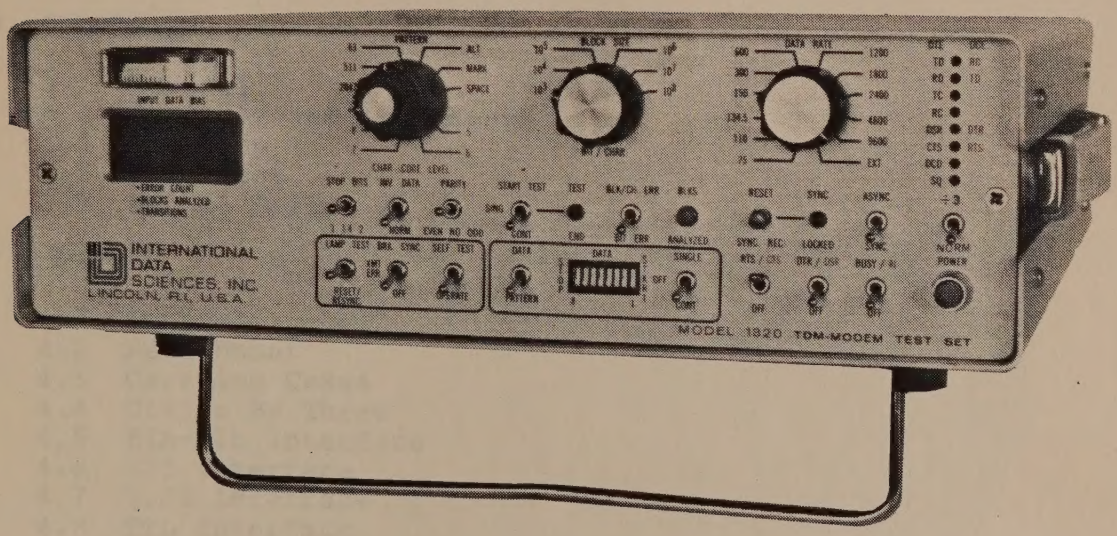

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1.0 INTRODUCTION

1.1 General

The IDS Model 1320 shown in Figure 1-1 is a portable, self-contained data test set designed to analyze the error rate of any digital transmission network. It can be used to test synchronous, asynchronous, or start/stop character-oriented systems such as time division multiplexers. Bit, character, and block error rates are determined by transmitting pseudo-random test patterns over the communications channel. These test patterns are statistically optimum and accurately simulate computer generated data. A start/stop character can be programmed and transmitted in either a single or continuous format.

The Model 1320 TDM-Modem Test Set (henceforth referred to as the test set) uses the latest state-of-the-art technology that operates faster and cooler than earlier Range Rider models.

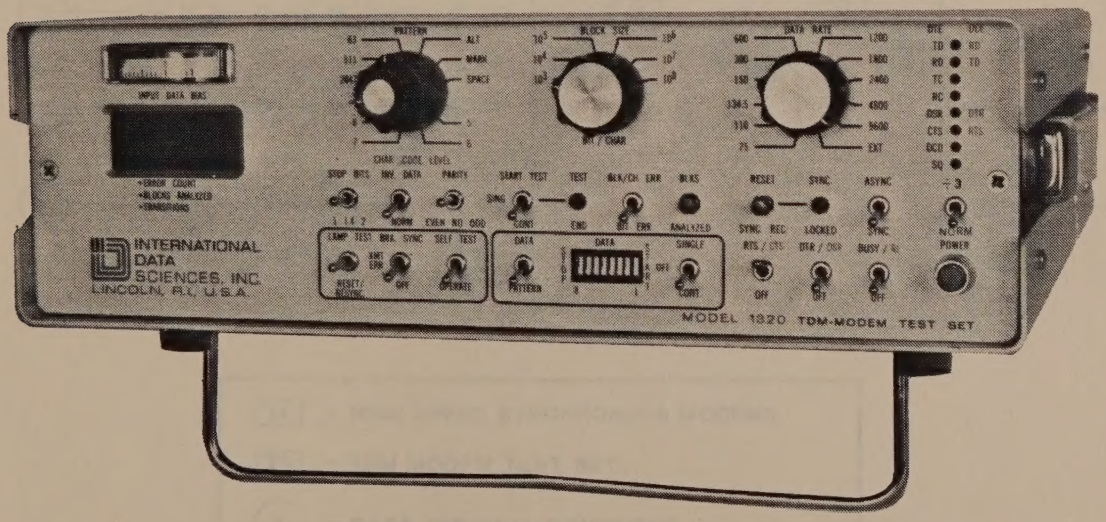
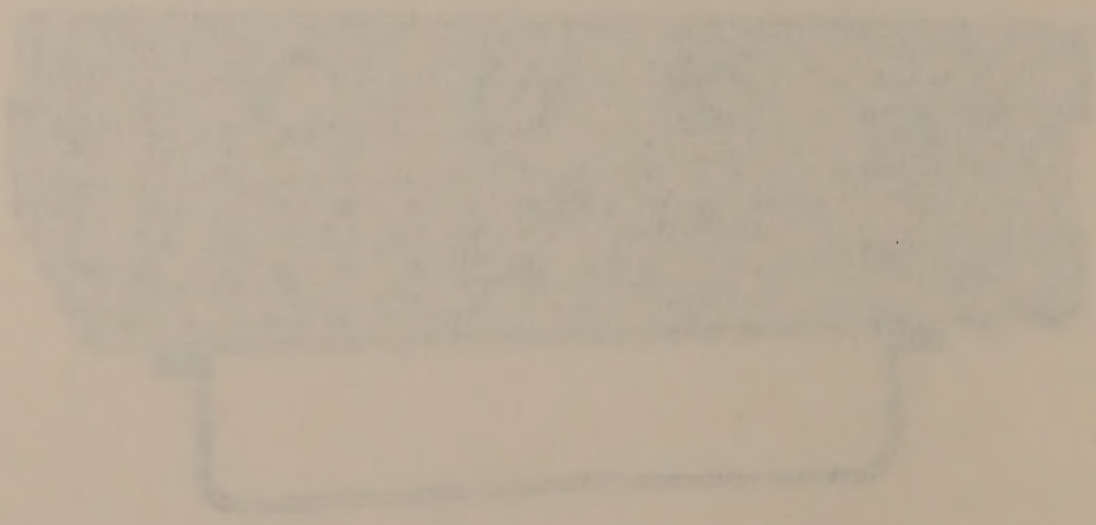


FIGURE 1-1. IDS MODEL 1320 TDM-MODEM TEST SET



1.2 Typical Test Configurations

The test set contains both a data transmitter and data receiver to allow simplex, half-duplex, and full-duplex testing of communication channels. Bit error rate tests (BERT) can be performed in either end-to-end or loopback configurations. Figure 1-2 shows a typical data communications system containing both asynchronous and synchronous modems and time division multiplexers (TDMs) with test sets indicated on Channels 2, 3, and 4 and the high-speed portion of the data link.

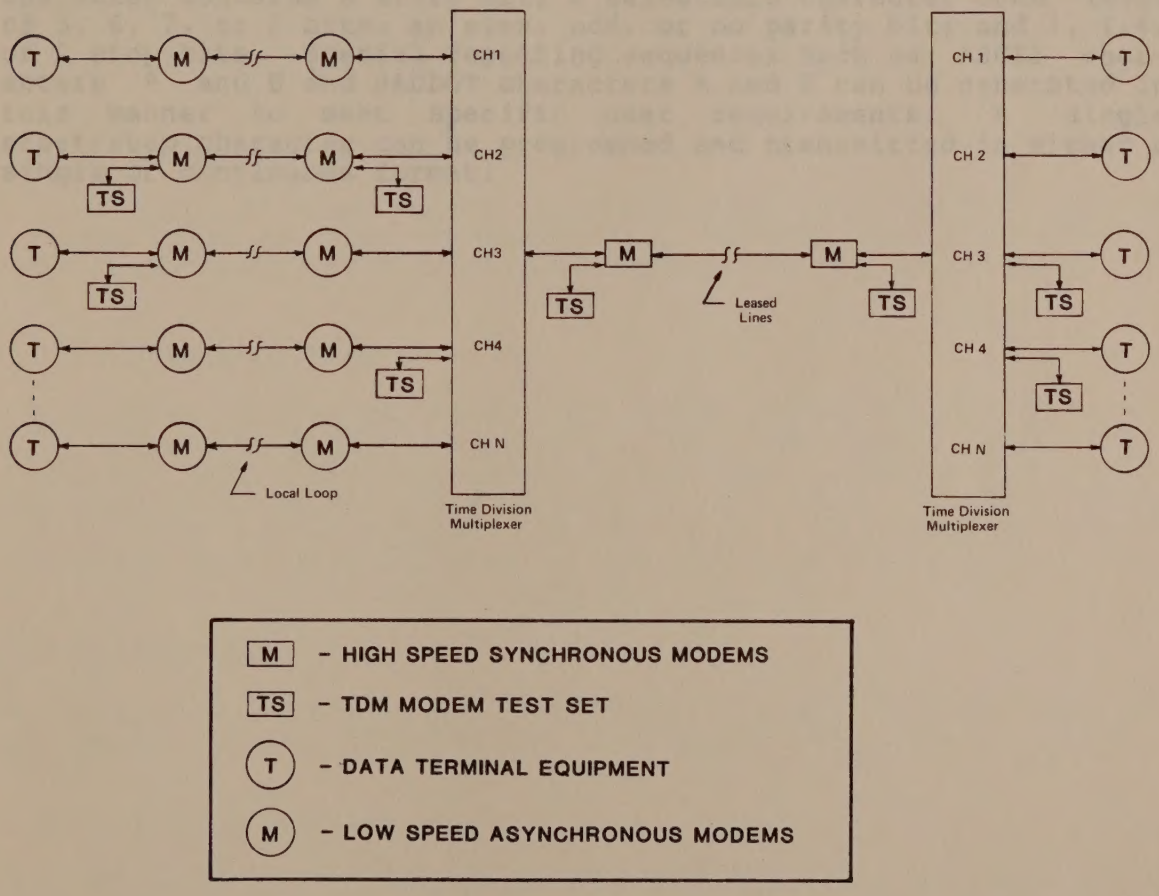
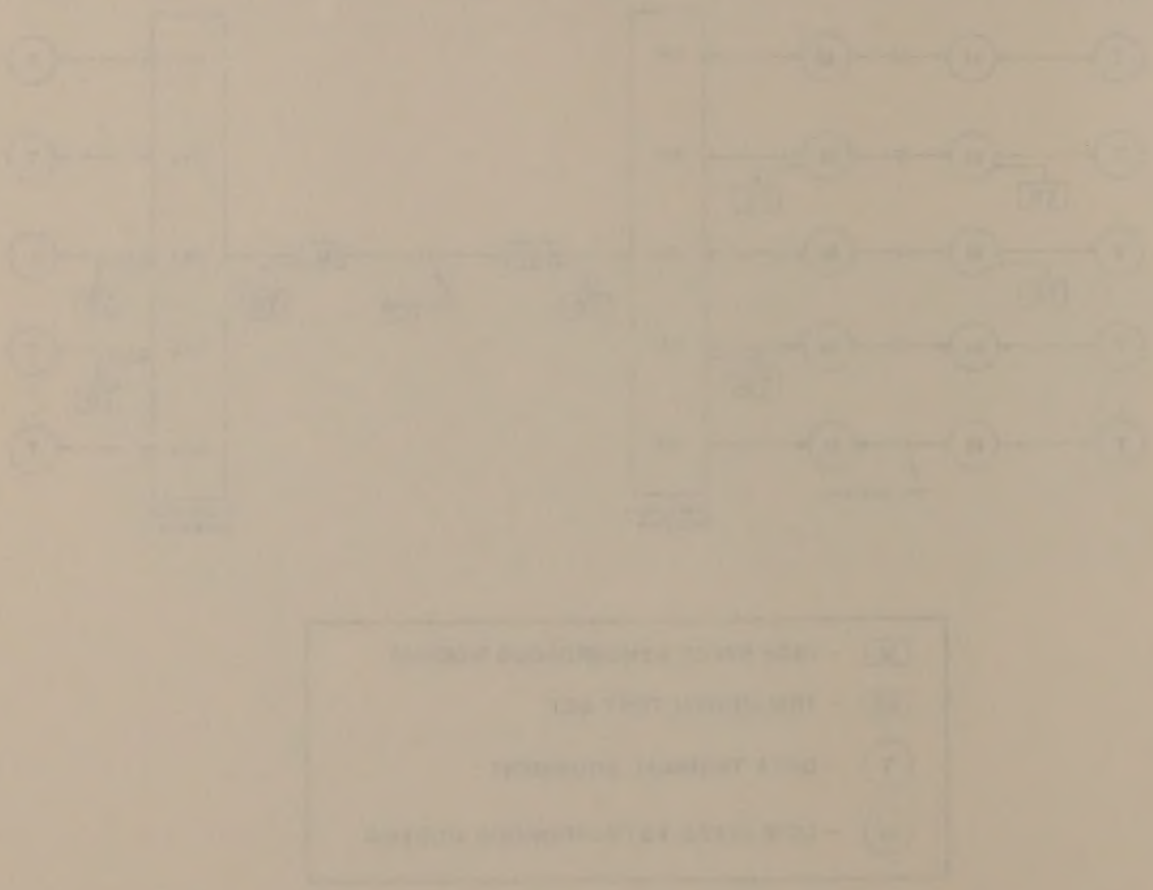


FIGURE 1-2. TYPICAL TEST CONFIGURATIONS



1.3 Features

Functional features of the test set are described in the following paragraphs.

1.3.1 Test Patterns

The transmitter can generate six basic data test patterns and their complements for transmission in either continuous or start/stop character format. These patterns include 63-, 511-, and 2047-bit pseudo-random sequences; an alternate mark/space pattern; a steady mark; and a steady space. The transmitted data pattern is under control of the RTS/CTS switch and is held to a mark when in the OFF position.

When data is generated in a start/stop character format, each character contains a start bit; a selectable character code level of 5, 6, 7, or 8 bits; an even, odd, or no parity bit; and 1, 1.4, or 2 stop bits. Special repeating sequences such as ASCII characters * and U and BAUDOT characters R and Y can be generated in this manner to meet specific user requirements. A single start/stop character can be programmed and transmitted in either a single or continuous format.

1.3.2 Data Rates

When externally timed for synchronous applications, the test set can operate at speeds up to 400,000 bps. For asynchronous applications and when providing timing to externally timed synchronous modems, a highly stable crystal-controlled oscillator provides a selection of the most commonly used data rates. These data rates include 75, 110, 134.5, 150, 300, 600, 1200, 1800, 2400, 4800, and 9600 bps. An option is available that allows the selected data rate to be divided by 3.

1.3.3 Error Rate Analysis

The receiver generates a true replica of the transmitted data pattern and compares it with the received data. Bit, character, or block errors are counted and displayed on the three-digit LED readout. Simultaneously, the total number of bits, characters, or blocks analyzed is also tallied and available for display. Blocks of bits or characters ranging from 10^3 to 10^8, or a single block of bits or characters can be selected for analysis.

1.3.4 Transition Detector

Steady mark and steady space signals generated by the test set can be used to detect mark-to-space and space-to-mark transitions. Line transitions are counted and displayed on the LED readout.

1.3.5 Interface Display

Eight front panel LEDs monitor the status of key EIA RS-232 interface signals. Signals monitored include transmitted data (TD), received data (RD), transmitter clock (TC), receiver clock (RC), data set ready (DSR), clear to send (CTS), data carrier detect (DCD), and signal quality detect (SQ). The LEDs are labeled according to whether the test set is used as a DTE or DCE.

1.3.6 Self-Test

A self-test feature allows the operator to verify proper test set operation without disconnecting it from the data link.

1.3.7 Printer Interface

An IDS Model 2010 Programable Digital Printer can be connected to the test set to obtain an unattended record of test results. The printer is interfaced through a standard rear panel connector.

1.4 Technical Specifications

1.4.1 Dimensions

Height:	4 inches	(10.2 cm)
Width:	12 7/8 inches	(32.7 cm)
Depth:	14 1/4 inches	(41.2 cm)

1.4.2 Weight

The test set weighs approximately 11 pounds, 12 ounces (5.32 Kg) uncrated.

1.4.3 Primary Power

The test set is switch selectable for 115 VAC, 60 Hz + or - 10% and 230 VAC, 50 Hz + or - 10% power input. Internal protection is provided by a 1 Amp, Slow Blow or a 1/2 Amp, Slow blow fuse, respectively. Power consumption is approximately 40 watts.

1.4.4 Environmental Conditions

Operating Temperature:	0^{o} - 50^{o} C.
Relative Humidity:	90%, non-condensing.

1.4.5 Interface

Conforms to EIA RS-232-C and CCITT V.24 specifications.

1.4.6 Data Format

Asynchronous: Continuous data or start/stop characters.
Synchronous: Continuous data pattern.

1.5 Options

Table 1-1 lists and describes options available for use with the test set. These options are further described in Section 4.0.

TABLE 1-1. OPTIONS

OPTION	DESCRIPTION
Rack Mount	Allows test set to be mounted in a standard 19-inch cabinet.
Carrying Cases	Allows heavy-duty handling of test set.
Divide by Three	Allows selected data rate to be divided by a factor of three (3).
EIA-MIL Interface	Allows test set to be switch selectable to operate with a standard RS-232 or MIL-188 interface.
303 Interface	Allows test set to operate with Bell 301/303 type interfaces.
V.35 Interface	Allows test set to operate with a CCITT V.35 interface.
TTL Interface	Allows test set to operate with a TTL interface.
TTY Interface	Allows test set to operate with a TTY interface.
RS-422/423 Interface	Allows test set to operate with a RS-422/423 interface.
External Clock	Provides clock rates of 40.8 Kbps, 48 Kbps, 50 Kbps, and 56 Kbps for operation with the 303 and V.35 optional interfaces.

NOTE: All optional interfaces and external clock sources are selected via a rear panel rotary switch.

2.0 INSTALLATION

2.1 General

Installation of the test set is based on the options being used and the specific application or intended use. This section provides information to satisfy general mechanical and electrical installation and strapping requirements. Field service personnel should become familiar with all installation procedures before attempting to install the test set. Upon completion of all installation requirements, refer to Section 3.0 for power-up and operation/test procedures.

2.2 Site Preparation

The installation area should be clean, well lighted, and free from extremes of temperature, humidity, appreciable shock, and vibration. A grounded AC outlet capable of furnishing primary power as specified in paragraph 1.4.3 should be located within 7 1/2 feet of the installation area.

2.3 Unpacking and Inspection

Before unpacking the test set, inspect the packing container for unusual damage. Then unpack the unit and inspect is for external damage such as scratches or dents and broken controls, indicators, and connectors. If physical damage is present, retain the packing material and contact the carrier immediately. Each test set has been thoroughly inspected prior to shipment.

2.4 Tools/Equipment/Materials Required

No special tools or equipment are required to install the test set. Any standard field service tool kit can be used.

2.5 Mechanical Installation

2.5.1 Desktop

The test set is a free-standing unit equipped with plastic feet and a metal bale. Use of the bale tilts the front of the test set upwards, providing a better view of the error count display and better access to front panel controls.

2.5.2 Rack Mount

A rack mount adaptor is optionally available for mounting the test set in a standard 19-inch wide EIA cabinet. This option is further described in paragraph 6.2.

2.6 Electrical Installation

2.6.1 AC Power Cord

AC power is supplied to the test set by a removable 7 1/2-foot line cord with a grounded 3-wire plug. The line cord mates with a receptacle at the rear of the unit (see Figure 2-1). Power requirements are specified in paragraph 1.4.3.

FIGURE 2-1. STANDARD REAR PANEL CONNECTORS

2.6.2 EIA Interface (To DCE, To DTE)

Two 25-pin connectors (labeled To DCE and To DTE) provide the interface for connecting the test set to the data communications equipment or data terminal equipment, respectively (see Figure 2-1). This interface conforms to the Electronic Industries Association (EIA) RS-232-C Standards and the Consultive Committee of International Telephone and Telegraph (CCITT) Standard V.24. Table 2-1 lists and describes the function of each signal conductor per EIA/CCITT specifications.

The test set is connected to the data interface via a six-foot standard 25-conductor EIA interface cable supplied with the unit. Note that the test set can only be connected to the DCE or DTE at any one time.

Electrical specifications for EIA interface signals are as follows:

a. Interface Output Drivers:

Data Rate - 400 Kbps, maximum.

Binary One - -6V + or - 0.5 volts.

Binary Zero - +6V + or - 0.5 volts.

Impedance - Less than 100 ohms for data and clock signals. Less than 1000 ohms for control signals.

Control Signals On, Space - +12V + or - 1 volt.

Control Signals Off, Mark - -12V + or - 1 volt.

Protection - Outputs are protected against shorting up to + or - 25 volts.

b. Interface Input Receivers:

Binary One - 2 volts to -25 volts.

Binary Zero - +2 volts to +25 volts.

Impedance - 3000 ohms to 7000 ohms.

Noise Immunity - + or - 2 volts with hysteresis.

Protection - + or - 25 volts without damage to receiver circuits.

2.6.3 Printer Interface

A female 25-pin connector located on the rear panel provides the interface for connecting the test set to a printer (see Figure 2-1). An IDS Model 2010 Programable Digital Printer can be used to obtain an unattended record of test results. The printer records the test set's error rate count, a channel identifier, and the time of day. A six-foot, 25-conductor EIA interface cable is supplied with the printer. Table 2-2 lists and describes the function of each interface signal conductor.

NOTE: For proper test set operation, the printer must be powered-up when connected to this interface.

TABLE 2-1. EIA/CCITT INTERFACE DESCRIPTION

PIN #	MNEMONIC NAME	DIRECTION		CIRCUIT		DESCRIPTION
		TO DTE	TO DCE	EIA	CCITT	
1	FG			AA	101	FRAME GROUND - This lead is an electrical equipment frame and power ground.
2	TD		→	BA	103	TRANSMITTED DATA - This lead carries the serial digital data transmitted from the DTE to the DCE.
3	RD	←		BB	104	RECEIVED DATA - This lead carries the serial digital data received at the DTE.
4	RTS		→	CA	105	REQUEST TO SEND - An "ON" condition on this lead is used to enable the local DCE for data transmission.
5	CTS	←		CB	106	CLEAR TO SEND - An "ON" condition on this lead indicates whether or not the DCE is ready to transmit data.
6	DSR	←		CC	107	DATA SET READY - An "ON" condition on this lead indicates that the local DCE is ready to process data and is not in a test, talk, or dial mode.
7	SG			AB	102	SIGNAL GROUND - This lead establishes the common ground reference potential for all circuits except frame ground on Pin 1.
8	DCD	←		CF	109	DATA CARRIER DETECT (Received Line Signal Detector) - This lead indicates that data from the remote location is being received and meets a suitable criteria established by the DCE manufacturer.
9	-					Not Used.
10	-					Not Used.
11	-					Not Used.
12	-					Not Used.
13	-					Not Used.
14	-					Not Used.
15	TC	←		DB	114	TRANSMITTER CLOCK - This lead is used to provide the DTE with signal element timing information.
16	-					Not Used.
17	RC	←		DD	115	RECEIVER CLOCK - This lead is used to provide the DTE with received signal element timing information.

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TABLE 2-1. EIA/CCITT INTERFACE DESCRIPTION (continued)

PIN #	MNEMONIC NAME	DIRECTION		CIRCUIT		DESCRIPTION
		TO DTE	TO DCE	EIA	CCITT	
18	-					Not Used.
19	-					Not Used.
20	DTR		→	CD	108.2	DATA TERMINAL READY - An "ON" condition on this lead indicates that the DTE is ready to be connected to the communication channel.
21	SQ	←		CG	110	SIGNAL QUALITY DETECT - This lead is used to indicate whether or not there is a high probability of an error in the received data.
22	RI	←		CE	125	RING INDICATOR - An "ON" condition on this lead indicates that a ringing signal is being received on the communication channel.
23	-					Not Used.
24	(TC)		→	DA	113	EXTERNAL TRANSMITTER CLOCK - This lead is used to provide the transmitting signal converter with signal element timing information.
25	BUSY		→	BELL 208A		BUSY - This lead is used for testing purposes by Telephone Company personnel. (Non-EIA designated).

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TABLE 2-2. PRINTER INTERFACE DESCRIPTION

#	SIGNAL NAME	SIGNAL FLOW	DESCRIPTION
1	Xmit Word Sync	To Printer	A positive going pulse at the beginning of each transmitted data pattern.
2	Data Error	To Printer	A negative going pulse indicates a bit or block has been received by the modem test set.
3	Clock Lost	To Printer	A normally high level which goes low whenever receive clock is absent.
4	BCD Bit 800	To Printer	Binary Coded Decimal (BCD) data is connected to these inputs. Normally the inputs are connected to a modem test set which represents the Error Counter Readout of the test set.
5	BCD Bit 400	To Printer	
6	BCD Bit 100	To Printer	
7	BCD Bit 200	To Printer	
8	BCD Bit 40	To Printer	
9	BCD Bit 80	To Printer	
10	BCD Bit 10	To Printer	
11	BCD Bit 20	To Printer	
12	BCD Bit 4	To Printer	
13	BCD Bit 8	To Printer	
14	BCD Bit 2	To Printer	
15	BCD Bit 1	To Printer	
16	Xmit Clock	To Printer	Transmitter Timing.
17	Reset Count	From Printer	This negative output level is used to reset the display counter of the modem test set.
18	Xmit Data	To Printer	Transmitted data pattern (±6V).
19	Sync Recovered	To Printer	A low level indicates the modem test set has recovered sync.
20	Received Data	To Printer	Received data pattern (±6V).
21	Signal Ground		
22	Received Clock	To Printer	
23	Receive Word Sync	To Printer	A positive going pulse at the beginning of each received data pattern.
24	Sync Lost	To Printer	A positive going pulse indicates the modem test set has lost sync.
25	Chassis Ground		

3.0 OPERATION

3.1 General

This section describes all front panel controls and indicators, and provides information on power-up and operation/test procedures. The operator should become familiar with all controls and indicators before attempting to operate the test set.

3.2 Controls and Indicators

Front panel controls and indicators are shown in Figure 3-1 and described in the following paragraphs.

3.2.1 ERROR COUNT, BLOCKS ANALYZED, TRANSITIONS

A three-digit LED display that provides a direct readout of the number of bit errors or characters or blocks received in error; the number of blocks of bits or blocks of characters analyzed; and the number of mark-to-space or space-to-mark transitions depending upon the setting of front panel controls. Overrange is indicated by a blinking display.

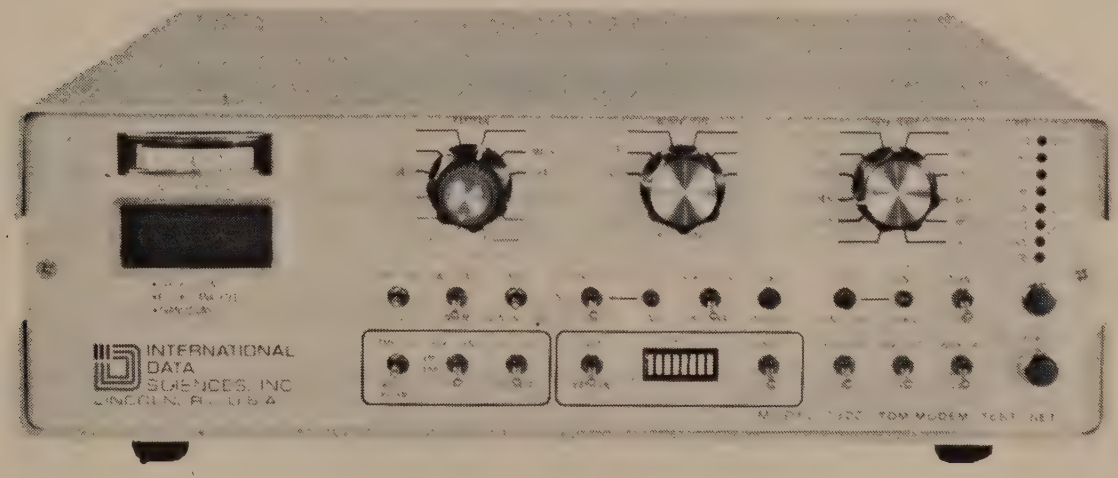


FIGURE 3-1. FRONT PANEL CONTROLS AND INDICATORS

3.2.2 RECEIVE DATA BIAS

This meter constantly monitors the mark or space bias distortion of the signal appearing on the received data (RD) line. The meter is calibrated in 10% increments ranging from 0% to 100% mark or 100% space bias distortion.

Patt - ALT

Char. Code level - ∞

Block Size - 10^6

Data Rate - EXT.

RTS/CTS - RTS

DTR/DSR - DTR

ASYNC/SYNC - SYNC

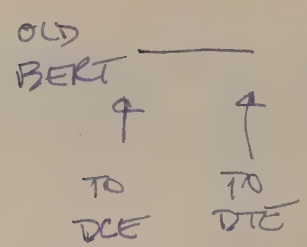
SINGLE/CONT - CONT

Par - NO

Data Patt. - Patt.

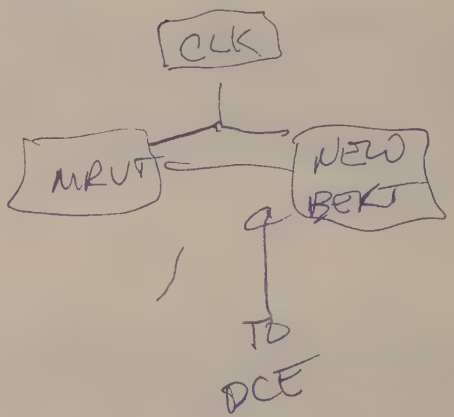
Xmit ERROR - OFF

(1) worked



DATA rate = 2400 (not EXT)

(2) failed



EXT CLK

or

DATA rate = xxx

3.2.3 PATTERN

A six-position rotary switch that allows the operator to select any one of six data patterns for transmission during the test. The 2047, 511, and 63 settings select pseudo-random sequences that repeat every 2047, 511, and 63 bits, respectively. The ALT, MARK, and SPACE settings select an alternate mark/space pattern, a steady mark, and a steady space, respectively.

3.2.4 CHAR CODE LEVEL

A five-position rotary switch, with settings of 5, 6, 7, 8, and ∞ (infinity), that determines how many bit positions in each character are allotted to data. The data contents of each character are determined by the setting of the PATTERN switch. When a 5, 6, 7, or 8-bit code level is selected, the data is character formatted with start and stop bits. In the ∞ position, the test set transmits continuous data bits.

3.2.5 BLOCK SIZE, BIT CHAR

A six-position rotary switch, with settings of 103, 104, 105, 106, 107, and 108 that partitions the received data into blocks of bits or blocks of characters, depending on the setting of the CHAR CODE LEVEL switch.

3.2.6 DATA RATE

A twelve-position rotary switch with eleven data rate selections ranging from 75 to 9600 bps and an EXT setting. The data rate selections are used when operating the test set with asynchronous systems or for selecting a transmitter clock to drive an externally timed synchronous modem. The EXT position is used when operating with synchronous systems at speeds up to 400,000 bps.

3.2.7 Interface Display

Eight LEDs monitor the status of key EIA RS-232 interface signals. Signals monitored include TD, RD, TC, RC, DSR, CTS, DCD, and SQ and are labeled according to whether the test set is used as a DTE or DCE.

3.2.8 STOP BITS

This three-position toggle switch selects the number of stop bits that follow the data and parity portion of each character transmitted as 1, 1.4, or 2 bits.

3.2.9 INV. DATA, NORM

This two-position toggle switch inverts all data, excluding start and stop characters, transmitted and received by the test set. The NORM position provides normal operation.

3.2.10 PARITY

This three-position toggle switch selects the parity bit that follows the data portion of each character. In the EVEN or ODD position, an even or odd parity bit is added based on the data contents of each character. The NO position eliminates the parity bit and the data is followed by the stop bit(s).

3.2.11 START TEST, SINGLE, CONT

This three-position toggle switch, having momentary action in the START TEST position, enables the test set to perform either on a SINGLE block of data or continuously (CONT). When momentarily held in the START TEST position, the test set will analyze a single block of data on a bit-by-bit or character-by-character basis.

3.2.12 TEST END

This LED is illuminated when the analysis of a single block of data has been completed. The LED is reset when the START TEST switch is enabled.

3.2.13 BLK/CH ERR, BIT ERR

This two-position toggle switch configures the test set to perform an error analysis on a block (BLK)/character (CH) or bit (BIT) basis.

3.2.14 BLKS. ANALYZED

When this pushbutton switch is depressed, the three-digit LED readout displays the total number of blocks of bits or characters that have been analyzed; thus allowing the bit, block, or character error rate to be determined.

3.2.15 RESET SYNC. REC.

When this pushbutton switch is depressed, the SYNC. LOCKED indicator is reset.

3.2.16 SYNC. LOCKED

This LED is illuminated to indicate that the test set is in synchronization with the received data. When this LED is blinking, it indicates that the receiver detected loss of synchronization during the test and has automatically resynchronized.

3.2.17 ASYNC., SYNC

This two-position toggle switch selects between asynchronous (ASYNC) or synchronous (SYNC) operation.

3.2.18 LAMP TEST, RESET/RESYNC

This three-position toggle switch has momentary-action in the LAMP TEST and RESET/RESYNC positions. When held in the LAMP TEST position, all front panel LEDs are illuminated for test purposes. When held in the RESET/RESYNC position, the LED readout is reset to "000", the test set will resynchronize, and the SYNC LOCKED indicator is reset.

3.2.19 BRK. SYNC., XMIT ERR, OFF

This three-position toggle switch has a momentary-action in the BRK. SYNC. position and allows the operator to interrupt normal test set operation for additional system analysis and self-test purposes. The OFF position enables normal operation. When in the XMIT ERR position, one error is inserted into each data pattern transmitted. Detection of the error verifies data link continuity and proper test set operation. When momentarily held in the BRK. SYNC. position, the test set becomes out of synchronization with the received data patterns. This provides a self-test of the loss of sync detection and auto-synchronization circuitry.

3.2.20 SELF TEST, OPERATE

This two-position toggle switch configures the test set for either SELF TEST or normal (OPERATE) operation. The self-test mode loops the transmitted data pattern directly into the receiver without having to disconnect the test set from the data link.

3.2.21 DATA, PATTERN

This two-position toggle switch configures the test set's transmission source as selected by the PATTERN switch, or as a programable data character selected by the DATA switch.

3.2.22 DATA

This DIP switch is used to configure the eight data bit locations of a start/stop character. The switch is labeled to indicate the position of the START and STOP bits, and least (1) and most (8) significant bit locations. Each switch is ON for a space (binary 0), or OFF for a mark (binary 1). The binary equivalent of the switch positions is labeled at the left of the Data switches. The setting of the CHAR CODE LEVEL switch determines how many data bits are used (starting with the least significant bit) and ignores the remaining bit positions for each start/stop character transmitted.

3.2.23 SINGLE, OFF, CONT.

This three-position toggle switch, having momentary action in the SINGLE position, controls transmission of the programed DATA character. When held in the SINGLE position, the test set transmits a single data character for error analysis. When switched to the CONT. position, the DATA character is transmitted in a continuous repeating format.

3.2.24 RTS/CTS

This two-position toggle switch controls the request to send (RTS) signal in the "TO DCE" interface, or the clear to send (CTS) signal in the "TO DTE" interface. The OFF position clamps the signal to a constant mark (binary 1).

3.2.25 DTR/DSR

This two-position toggle switch controls the data terminal ready (DTR) signal in the "TO DCE" interface, or the data set ready (DSR) signal in the "TO DTE" interface. The OFF position clamps the signal to a constant mark (binary 1).

3.2.26 BUSY/RI

This two-position toggle switch controls the BUSY signal in the "TO DCE" interface, or the ring indicator (RI) signal in the "TO DTE" interface. The OFF position clamps the signal to a constant mark (binary 1).

3.2.27 POWER

This pushbutton switch energizes the unit and initializes the counter and sync status circuitry.

3.3 Power-Up

The test set is powered-up by actuation of the POWER switch.

CAUTION: Before attempting to power-up the unit, assure that it has been switched to the proper line voltage.

3.4 Self-Test

A self-test feature allows the operator to verify proper test set operation without disconnecting it from the data link. By switching to SELF TEST, the unit is configured to loop the transmitted data pattern directly into the receiver input.

While in he SELF TEST mode, switching to XMIT ERR enables one error to be inserted into each data pattern transmitted. Detection of these errors verify proper test set operation.

In addition, by momentarily actuating the BRK. SYNC. switch, the receiver is forced to become out of synchronization with the transmitted test pattern. The loss of sync circuitry detects this failure and turns off the SYNC LOCKED LED. The test set then automatically resynchronizes and triggers the SYNC LOCKED LED blinking. Note that the SYNC LOCKED LED remains blinking until reset by the RESET SYNC. REC. or the RESET/RESYNC switch.

NOTE: This comprehensive self-test verifies proper operation of RS-232 and MIL-188 interfaces only. If the test set contains other optional interfaces, the rear panel INTERFACE SELECT switch must be set in either the RS-232 or MIL-188 positions.

3.5 Normal Operation

The test set can operate in a variety of asynchronous and synchronous applications. To ensure normal operation, the user must be familiar with various valid combination settings of the ASYNC-SYNC, DATA RATE, and CHAR CODE LEVEL switches. Table 3-1 lists these settings and describes the resultant test set operation. Note that for asynchronous operation an EXT data rate selection is not valid. Likewise, synchronous operation requires an CHAR CODE LEVEL selection for proper operation.

TABLE 3-1. ASYNC-SYNC CONFIGURATIONS

ASYNC-SYNC SELECTION	DATA RATE SELECTION	CHAR CODE LEVEL SELECTION	RESULTANT OPERATION
ASYNC	Not EXT	∞	Asynchronous operation; data in continuous format.
ASYNC	Not EXT	Not ∞	Asynchronous operation; data in start/stop character format.
ASYNC	EXT	Any	Invalid combination; test set inoperative.
SYNC	Not EXT	∞	Synchronous operation; data in continuous format. Transmit Clock supplied to modem at selected data rate.
SYNC	EXT	∞	Synchronous operation; data in continuous format. Modem supplies all timing.
SYNC	Any	Not ∞	Invalid combination; test set inoperative.

4.0 OPTIONS

4.1 General

The following paragraphs of this section describe each option available for the test set.

4.2 Rack Mount

A rack mount adaptor is available for mounting the test set in a standard 19-inch wide EIA cabinet. This option consists of a window-frame type front panel measuring 5 1/4 inches high by 19 inches wide (13.3 cm H x 48.3 cm W) with 25-pin connectors mounted at both sides of the window opening (see Figure 4-1). These connectors are labeled TO DTE and TO DCE and are cabled to their respective rear panel connectors. The rack mount adaptor is secured to the unit by side panels.

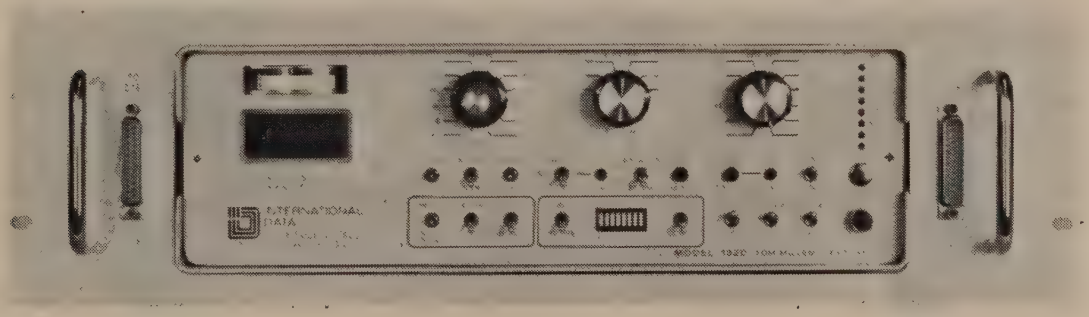


FIGURE 4-1. RACK MOUNT ADAPTOR

4.3 Carrying Cases

Two types of carrying cases are available for the test set. These carrying cases are described in the following paragraphs.

4.3.1 Model CA-1320

The Model CA-1320 carrying case is available for heavy duty handling of the test set. This aluminum case is internally lined with a foam insert contoured to the test set. A compartment for the line cord and interface cable is also provided. It can be locked and shipped with complete safety as airline luggage.

4.3.2 Model CP-1320

The Model CP-1320 carrying case is designed for lighter duty handling of the test set. This polyproplylene injected molded case is also internally lined with a foam insert contoured to the test set and has a cut-out for the line cord and interface cable.

4.4 Divide By Three

This option allows the operator to divide the selected data rate (except EXT) by a factor of three (3). A two-position toggle switch labeled -3 and NORM controls this function. This switch is installed above the POWER switch on the front panel as shown in Figure 4-2. Not applicable to optional data rates.

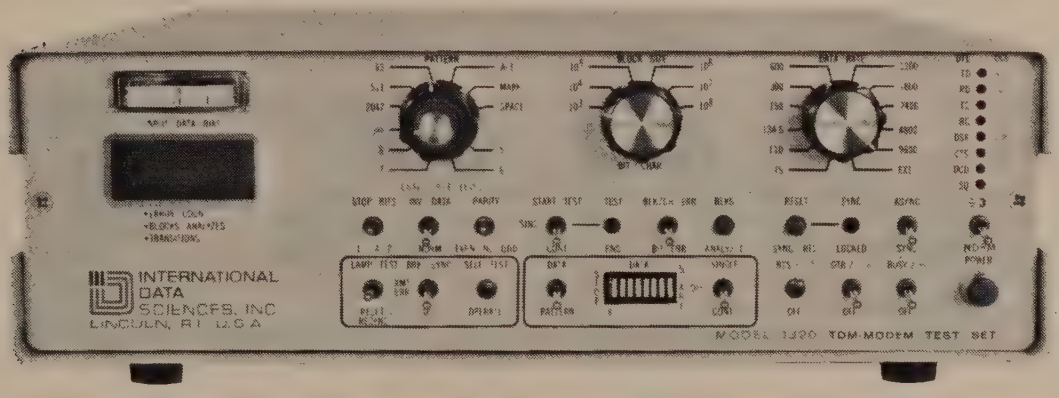


FIGURE 4-2. DIVIDE BY THREE OPTION

4.5 EIA-MIL Interface

4.5.1 Description

This option allows the test set to operate with the standard EIA RS-232 or MIL-188 interface through the same rear panel connectors. The option is available in two configurations. When this is the only option utilized, a two-position toggle switch labeled MIL and EIA controls this function. This switch is installed above the POWER switch on the front panel (in the same location utilized by the Divide By Three (-3) option). When the -3 option or other optional interfaces are utilized, the optional rear panel assembly is installed and a rotary switch is provided to select the desired interface. MIL-188 pin assignments are the same as described for the EIA RS-232 interface (refer to Table 2-2).

4.5.2 Electrical Specifications

Data Rate - 200 Kbps, maximum.

Binary One - +6V + or - 0.5V.

Binary Zero - -6V + or - 0.5V.

Driver Impedance (Z_{out}) - < 100 ohms for data and clocks;
< 1000 ohms for control signals.

Receiver Impedance (Z_{in}) - 6000 ohms, minimum.

Receiver Noise Immunity - + or - 0.6V with hysteresis.

Receiver Protection - + or - 25V without damage.

4.6 303 Interface

4.6.1 Description

This option allows the test set to operate with the Bell 301/303 Current Interface. A male 25-pin connector wired to a plug-in P.C. board provides this interface. The interface connector is installed on an optional rear panel assembly as shown in Figure 4-3. Table 4-1 lists and describes the function of each pin assignment. A rear panel rotary switch labeled INTERFACE SELECT configures the test set to operate through the selected interface.

A six-foot, 15-conductor cable, terminated with a female 25-pin connector and a male 12-pin Burndy connector, is provided to interconnect the test set to the data interface (see Figure 4-4).

FIGURE 4-3. OPTIONAL REAR PANEL INTERFACE CONNECTORS

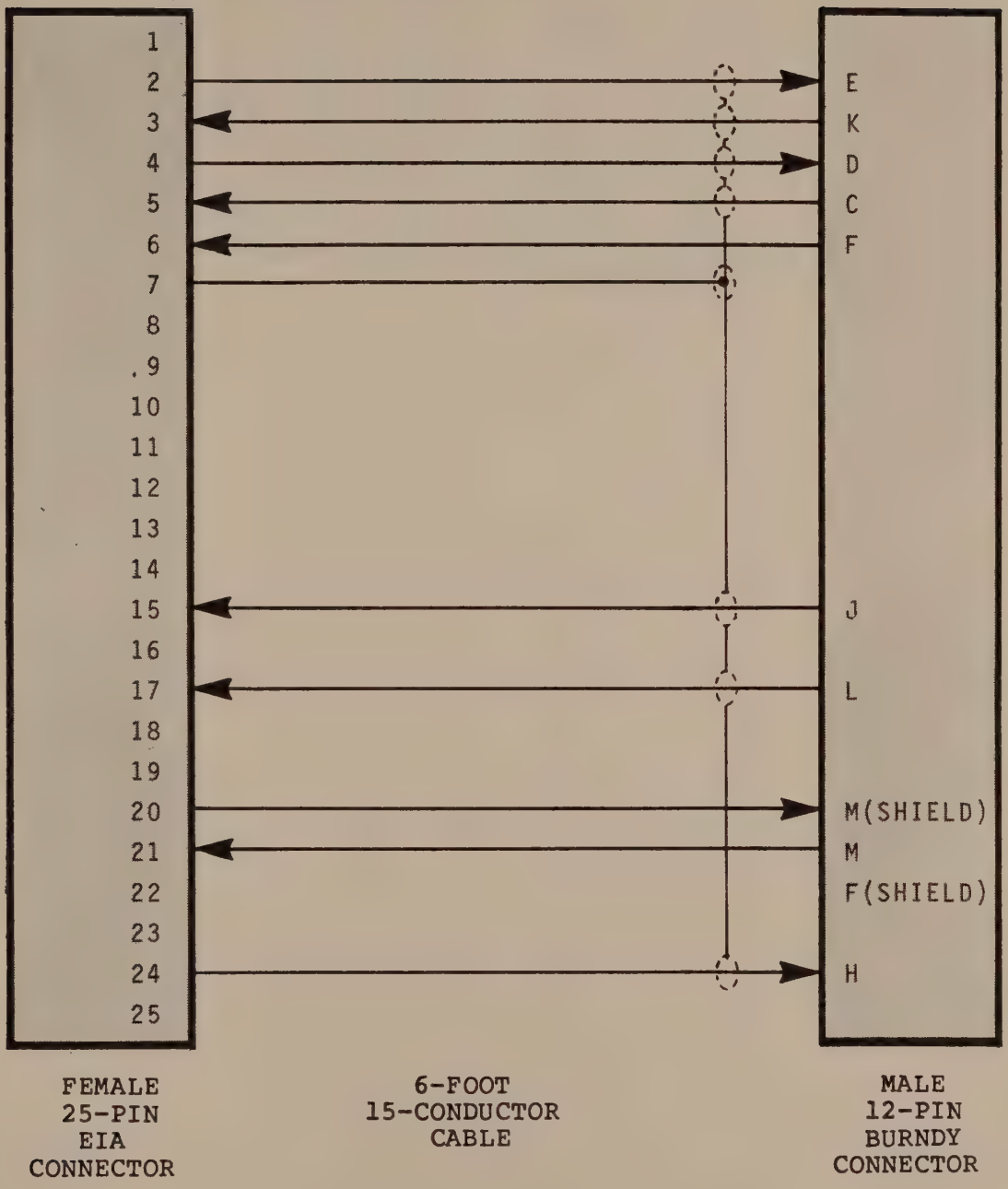


FIGURE 4-4. 303 Interface Adaptor Cable

4.6.2 Electrical Specifications

Data Rate - 1.0 Mbps, maximum.

Binary One (1), Mark, Off - < 5 mA.

Binary Zero (0), Space, On - > 23 mA.

Receiver Impedance (Z_{in}) - 100 ohms + or - 5%.

Open Circuit - Receiver assumes an OFF or Mark-Hold condition.

TABLE 4-1. 303 INTERFACE DESCRIPTION

PIN #	MNEMONIC NAME	DIRECTION		FUNCTION
		TO DTE	TO DCE	
1	-			NOT USED
2	SD		→	SEND DATA
3	RD	←		RECEIVE DATA
4	RS		→	REQUEST TO SEND
5	CS	←		CLEAR TO SEND
6	DSR	←		DATA SET READY
7	SG			SIGNAL GROUND
8	-			NOT USED
9	-			NOT USED
10	-			NOT USED
11	-			NOT USED
12	-			NOT USED
13	-			NOT USED
14	-			NOT USED
15	SCT	←		SERIAL CLOCK TRANSMIT
16	-			NOT USED
17	SCR	←		SERIAL CLOCK RECEIVE
18	-			NOT USED
19	-			NOT USED
20	DTR		→	DATA TERMINAL READY
21	AGC	←		AUTOMATIC GAIN CONTROL
22	-			NOT USED
23	-			NOT USED
24	SCTE		→	SERIAL CLOCK XMIT EXTERNAL
25	-			NOT USED

TABLE 4-2. V.35 INTERFACE DESCRIPTION

PIN #	MNEMONIC NAME	DIRECTION		FUNCTION
		TO DTE	TO DCE	
1	FG			FRAME GROUND
2	SD (A)		→	SEND DATA (SIGNAL A)
3	RD (A)	←		RECEIVED DATA (SIGNAL A)
4	SD (B)		→	SEND DATA (SIGNAL B)
5	RD (B)	←		RECEIVED DATA (SIGNAL B)
6	DSR	←		DATA SET READY
7	SG			SIGNAL GROUND
8	-			NOT USED
9	RTS		→	REQUEST TO SEND
10	CTS	←		CLEAR TO SEND
11	-			NOT USED
12	-			NOT USED
13	-			NOT USED
14	SCT (B)	←		SER. CLK. XMIT (SIG. B)
15	SCT (A)	←		SER. CLK. XMIT (SIG. A)
16	SCR (B)	←		SER. CLK. RECEIVE (SIG. B)
17	SCR (A)	←		SER. CLK. RECEIVE (SIG. A)
18	-			NOT USED
19	-			NOT USED
20	DTR		→	DATA TERMINAL READY
21	-			NOT USED
22	-			NOT USED
23	-			NOT USED
24	SCTE (A)		→	SER. CLK. XMIT EXT. (SIG. A)
25	SCTE (B)		→	SER. CLK. XMIT EXT. (SIG. B)

4.7 V.35 Interface

4.7.1 Description

This option allows the test set to operate with the CCITT V.35 interface. A male 25-pin connector wired to a plug-in P.C. board provides this interface. The interface connector is installed on an optional rear panel assembly (refer to Figure 4-3). Table 4-2 lists and describes the function of each pin assignment. A rear panel rotary switch labeled INTERFACE SELECT configures the test set to operate with the selected interface.

A six-foot 25-connector cable, terminated with a female 25-pin EIA connector and a male 34-pin Winchester connector, is provided to interconnect the test set to the data interface (see Figure 4-5).

4.7.2 Electrical Specifications

Data Rate - 1.0 Mbps, maximum.

Binary One - Output A negative with respect to output B.

Binary Zero - Output A positive with respect to output B.

Levels - + or - 1.1V + or - 0.1V.

Rise & Fall Time - Greater than 40 nanoseconds when measured between 10% and 90% of waveform rise and fall.

Impedance - 100 ohms + or - 1% balanced; 150 ohms + or - 1% with respect to ground with A and B shorted together.

Driver DC Offset - 0V + or - 0.2V for each output with respect to ground.

Driver Protection - Short circuit protected outputs to ground or to each other.

Receiver Sensitivity - + or - 10 millivolts, maximum.

Receiver DC Offset - + or - 0.6V, maximum.

Receiver Protection - + or - 10V without damage.

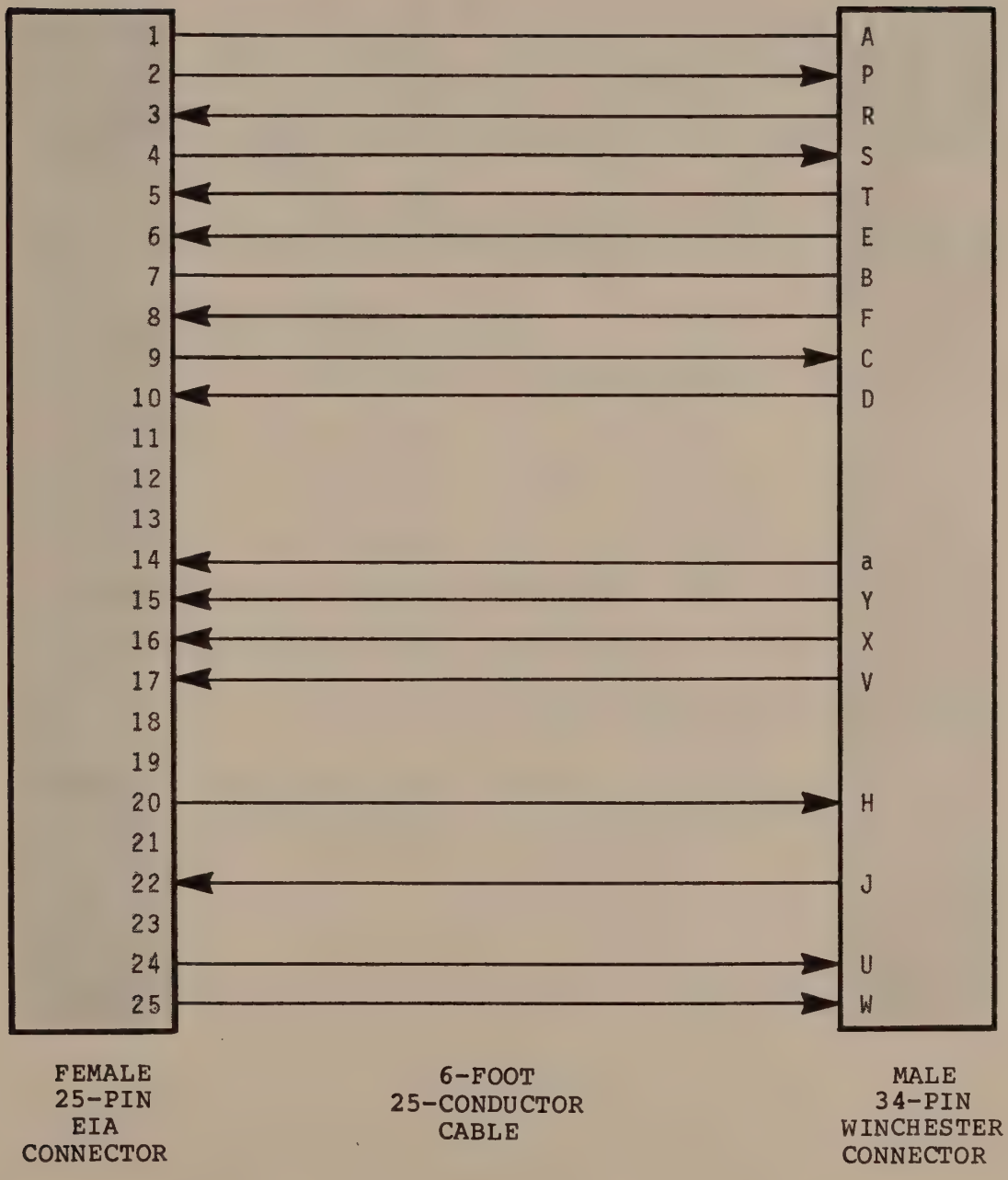


Figure 4-5. V.35 Interface Adaptor Cable

4.8 TTL Interface

4.8.1 Description

This option allows the test set to operate with a TTL interface. A male 25-pin connector wired to a plug-in P.C. board provides this interface. The interface connector is installed on an optional rear panel (refer to Figure 4-3). A rear panel rotary switch labeled INTERFACE SELECT configures the test set to operate with the selected interface. Table 4-3 lists and desoribes the function of each pin assignment.

The test set is connected to the data interface via a six-foot, standard 25-conductor EIA interface cable supplied with the unit.

4.8.2 Electrical Specifications

Data Rate - 1.0 Mbps, maximum.

Binary One (Driver) - 5V + or - .2V.

Binary One (Receiver) - Greater than 1.5V.

Binary Zero (Driver) - 0V + or - 0.7V.

Binary Zero (Receiver) - Less than 1.1V.

Driver Impedance (Z_{out}) - 125 ohms + or - 5%.

Driver Protection - Output protected against short circuit to ground.

Receiver Impedance (Z_{in}) - Greater than 5.5K ohms.

Receiver Protection - -1.5V to 5.5V.

TABLE 4-3. TTL INTERFACE DESCRIPTION

PIN #	MNEMONIC NAME	DIRECTION		FUNCTION
		TO DTE	TO DCE	
1	FG			FRAME GROUND
2	TD		→	TRANSMIT DATA
3	RD	←		RECEIVE DATA
4	RTS		→	REQUEST TO SEND
5	-			NOT USED
6	-			NOT USED
7	SG			SIGNAL GROUND
8	-			NOT USED
9	-			NOT USED
10	-			NOT USED
11	-			NOT USED
12	-			NOT USED
13	-			NOT USED
14	-			NOT USED
15	TC	←		TRANSMIT CLOCK
16	-			NOT USED
17	RC	←		RECEIVE CLOCK
18	-			NOT USED
19	-			NOT USED
20	DTR		→	DATA TERMINAL READY
21	-			NOT USED
22	-			NOT USED
23	-			NOT USED
24	SCTE		→	SERIAL CLOCK XMIT EXTERNAL
25	-			NOT USED

4.9 TTY Interface

4.9.1 Description

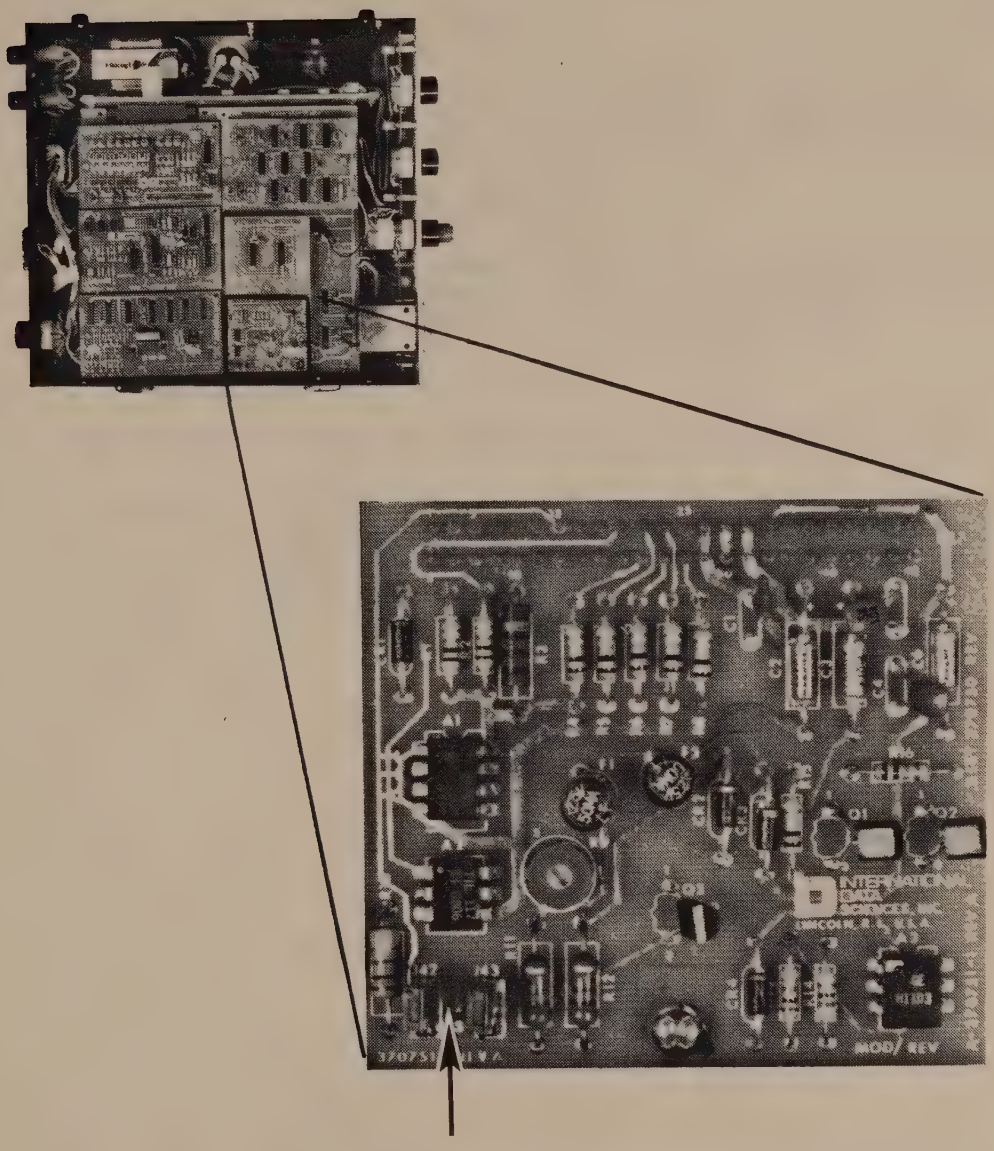
This option allows the test set to operate with teletypewriter (TTY) equipment using a 20 or 60 mA current loop interface. A 4-screw terminal strip wired to a plug-in P.C. board provides this interface. The terminal strip is installed on an optional rear panel (refer to Figure 4-3). A rear panel rotary switch labeled INTERFACE SELECT configures the test set to operate with the desired interface.

The terminal strip has two screws labeled TD for the connection of transmit data lines, and two screws labeled RD for the connection of receive data lines. Each screw is also labeled to designate the connection of the tip (T) and ring (R) leads. A 4-conductor cable, terminated at each end with high pressure fork lug connectors is provided to interconnect the test set to the data interface.

4.9.2 Strapping

The TTY interface P.C. board can be strapped to supply the current loop source (if required). These straps are accessible by removing the top cover of the test set. Strapping is accomplished by positioning jumper plugs over terminal pins found at various locations on the P.C. board (see Figure 4-6).

Terminal pins J42 and J43 configure the interface for active or passive operation. In active operation, the test set provides the current loop source. In passive (normal) operation, the system supplies the current loop source. Positioning a jumper plug over J42-1 an J42-2, and over J43-1 and J43-2 configures active operation. Positioning a jumper plug over J42-2 and J42-3, and over J43-2 and J43-3 configures passive operation.



TERMINAL PINS
J42 AND J43

Figure 4-6. TTY Strap Locations

4.9.3 Electrical Specifications

Data Rate - 9600 bps, maximum.

Loop Current - 20 mA (active or internal loop).
20 mA or 60 mA (passive or external loop) into a 100 ohm load.

Loop Voltage - 150 volts, maximum.

Mark - Current greater than 10 mA (20 mA loop) into a 100 ohm load; current greater than 30 mA (60 mA loop) into a 100 ohm load.

Space - No current flow.

Isolation - Opto-isolated between loop and TTL levels.

Protection - Inputs and outputs of TTY receivers and transmitters are diode protected against reverse polarity; internal loop source fuse protected.

4.10 RS-422/423 Interface

4.10.1 Description

This option allows the test set to operate with the EIA Rs-422/423 interface. A male 25-pin connector wired to a plug-in P.C. board provides this interface. The interface connector is installed on an optional rear panel assembly (refer to Figure 4-3). Table 4-4 lists and describes the function of each pin assignment. A rear panel rotary switch labeled INTERFACE SELECT configures the test set to operate with the selected interface.

A six-foot 25-conductor cable, terminated with a female 25-pin EIA connector and a male 37-pin EIA connector, is provided to interconnect the test set to the data interface (see Figure 4-7).

4.10.2 Strapping

The RS-422/423 interface P.C. board provides strapping to allow terminal timing (TT, Pins 24 and 25) to be derived from the standard data rate selections or from the external clock option (if installed). These straps are accessible by removing the top cover of the test set. Strapping is accomplished by positioning jumper plugs over terminal pins and setting DIP switches found at various locations on the P.C. board (see Figure 4-8).

Strap selections are also provided to allow data and timing signals to operate in either single ended or balanced modes. All control signals are single ended. Receiver terminating resistors can be selected for balanced operation based on the specific operating environment. RS-422/423 strap selections are described separately in the following paragraphs.

4.10.2.1 TT Source

Terminal Pins J44-1 through J44-2 and DIP switch S1-8 configure the TT source. Positioning the jumper plug over J44-1 and J44-2, and switching S1-8 to the OFF position, disables TT. Positioning the jumper plug over J44-2 and J44-3, with S1-8 in the OFF position, configures TT to be derived from the standard data rate selections. Positioning the jumper plug over J44-3 and J44-4, and switching S1-8 to the ON position (see Figure 4-9), configures TT to be derived from the external clock option.

TABLE 4-4. RS-422/423 INTERFACE DESCRIPTION

PIN #	MNEMONIC NAME	DIRECTION		FUNCTION
		TO DTE	TO DCE	
1				SHIELD
2	SD(A)		→	SEND DATA (SIGNAL A)
3	RD(A)	←		RECEIVE DATA (SIGNAL A)
4	SD(B)		→	SECONDARY SEND DATA (SIGNAL B)
5	RD(B)	←		SECONDARY RECEIVE DATA (SIGNAL B)
6	DM	←		DATA MODE
7	SG			SIGNAL GROUND
8	-			NOT USED
9	RS		→	REQUEST TO SEND
10	CS	←		CLEAR TO SEND
11	-			NOT USED
12	-			NOT USED
13	-			NOT USED
14	ST(B)	←		SEND TIMING (SIGNAL B)
15	ST(A)	←		SEND TIMING (SIGNAL A)
16	RT(B)	←		RECEIVE TIMING (SIGNAL B)
17	RT(A)	←		RECEIVE TIMING (SIGNAL A)
18	-			NOT USED
19	-			NOT USED
20	TR		→	TERMINAL READY
21	SQ	←		SIGNAL QUALITY
22	-			NOT USED
23	-			NOT USED
24	TT(A)		→	TERMINAL TIMING (SIGNAL A)
25	TT(B)		→	TERMINAL TIMING (SIGNAL B)

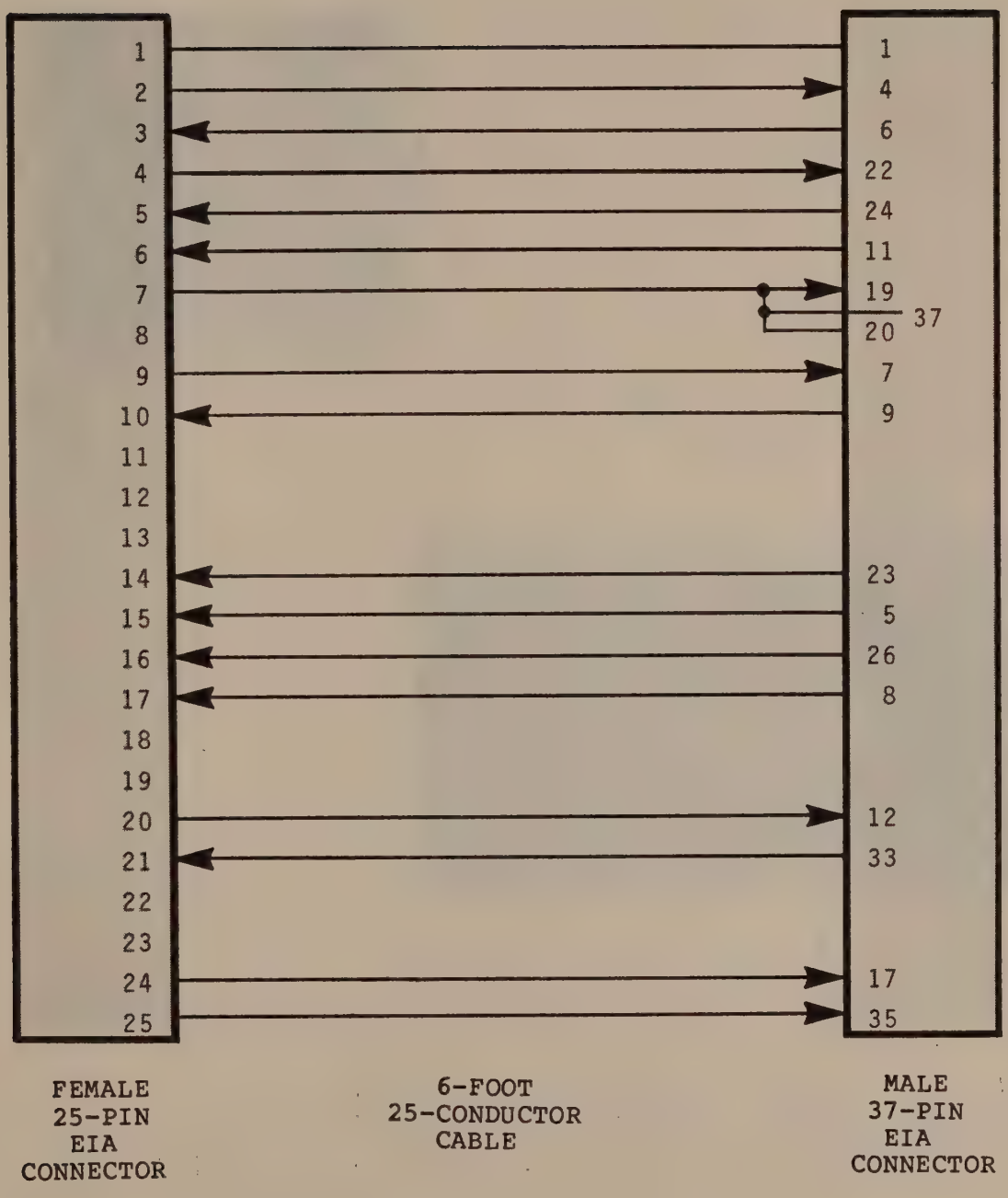


Figure 4-7. RS-422/423 Interface Adaptor Cable

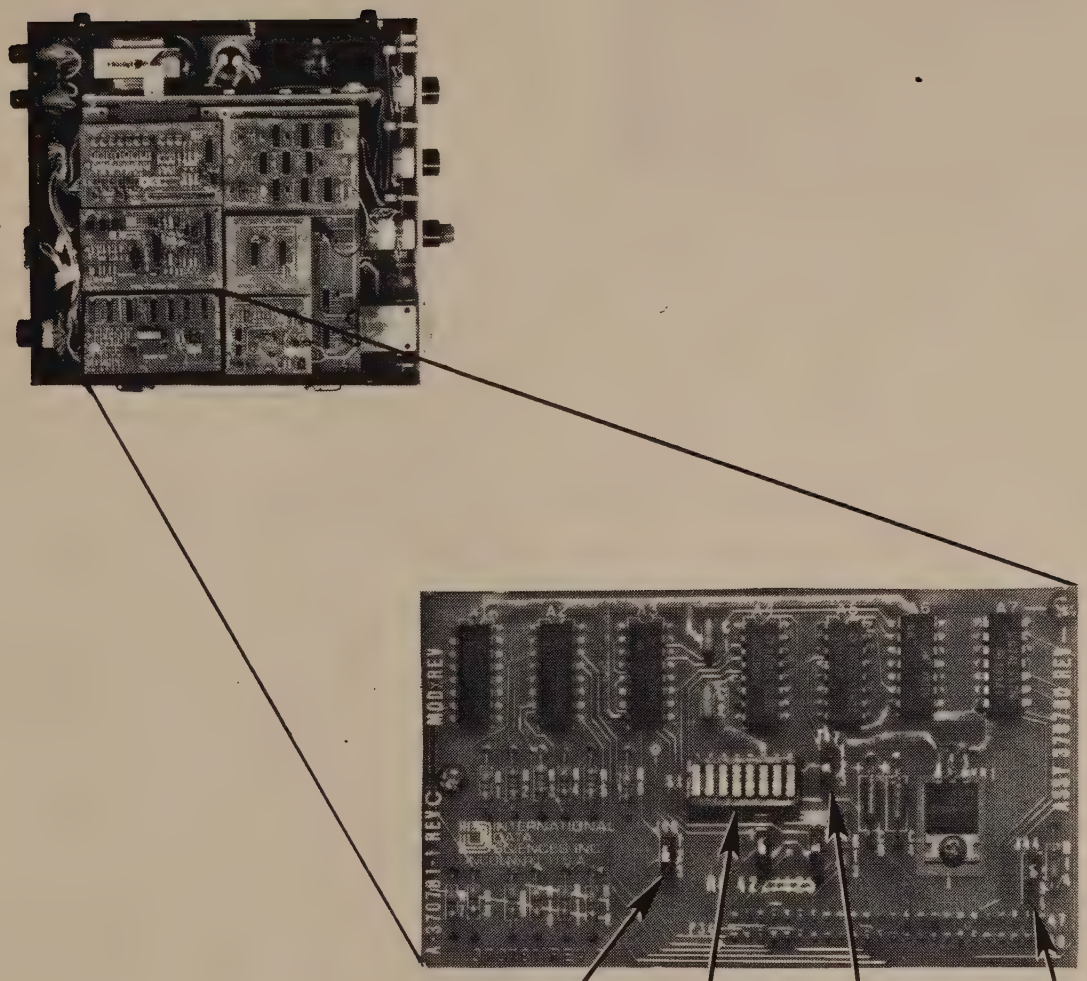
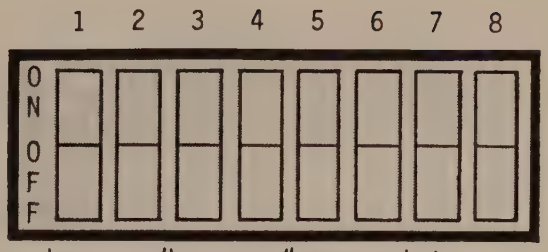


Figure 4-8. RS-422/423 Strap Locations



RD CONFIGURATIONS		
FUNCTION	1	2
Balanced	OFF	OFF
Single Ended	ON	OFF
120 Ohm Termination	OFF	ON

RT CONFIGURATIONS		
FUNCTION	3	4
Balanced	OFF	OFF
Single Ended	OFF	ON
120 Ohm Termination	ON	OFF

ST CONFIGURATIONS		
FUNCTION	5	6
Balanced	OFF	OFF
Single Ended	OFF	ON
120 Ohm Termination	ON	OFF

NOT USED

TT SOURCE
(Refer to paragraph 4.10.2.1)

Figure 4-9. DIP Switch S1 Strapping

4.10.2.2 Interface Configurations

DIP switch S1, and Terminal Pins J47 - J50 control various RS-422/423 interface configurations. DIP switch S1 selects receive data (RD), receive timing (RT), and send timing (ST) configurations. Figure 4-9 illustrates the strap positions and describes their functions.

Terminal Pins J47, J50, and J48, J49 select send data (SD) and terminal timing (TT) configurations, respectively. Positioning jumper plugs over Pins J47-1,2 and J50-1,2 selects a balanced SD output. Positioning jumper plugs over Pins J47-2,3 and J50-2,3 selects a single ended SD output. Likewise, positioning jumper plugs over Pins J48-1,2 and J49-1,2 selects a balanced TT output; and positioning jumper plugs over J48-2,3 and J49-2,3 selects a single ended TT output.

4.10.3 Electrical Specifications

Data Rate - 1.0 Mbps, maximum.

Binary One, Mark, Off - A negative with respect to B.

Binary Zero, Space, On - A positive with respect to B.

Driver Impedance (Z_{out}) - 100 ohms $\pm$ 1% balanced,
50 ohms $\pm$ 1% single ended.

Rise and Fall Time - Greater than 20 na when measured between 10% and 90% of rise or fall.

Driver DC Offset - 0V $\pm$ 0.5V balanced,
0V $\pm$ 0.25V single ended.

Driver Protection - Outputs short circuit protected to ground or each other (150 mA maximum).

Receiver Sensitivity - $\pm$ 200 mv maximum balanced,
$\pm$ 400 mv maximum single ended.

Receiver Impedance (Z_{in}) - 4000 ohm minimum balanced,
2000 ohm minimum single ended.

Receiver DC Offset - +7V maximum for proper operation.

Receiver Protection - $\pm$ 15V maximum without damage to receiver circuits.

4.11 External Clock

4.11.1 Description

This option provides an additional external transmit timing source for operation with the 303, V.35, RS-422/423, and W.U.L.L. interfaces. The external clock is configured as a plug-in P.C. board that is strap selectable for 40.8 Kbps, 48 Kbps, 50 Kbps, and 56 Kbps operation. The INTERFACE SELECT switch selects the external clock source for 303 and V.35 when switched to the 303/CLK and V.35/CLK positions, respectively. RS-422/423 and W.U.L.L. require additional internal strapping.

4.11.2 Strapping

The external clock P.C. board is strap selectable to operate at one of four rates. These straps are accessible by removing the top cover of the test set. Strapping is accomplished by positioning jumper plugs over terminal pins labeled E1 through E6 on the P.C. board (see Figure 4-10). Table 4-5 lists and describes external clock strapping configurations.

TABLE 4-5. EXTERNAL CLOCK STRAPPING

CLOCK RATE	STRAP POSITION
40.8 Kbps	E5 - E6
48 Kbps	E4 - E5
50 Kbps	E2 - E3
56 Kbps	E1 - E2

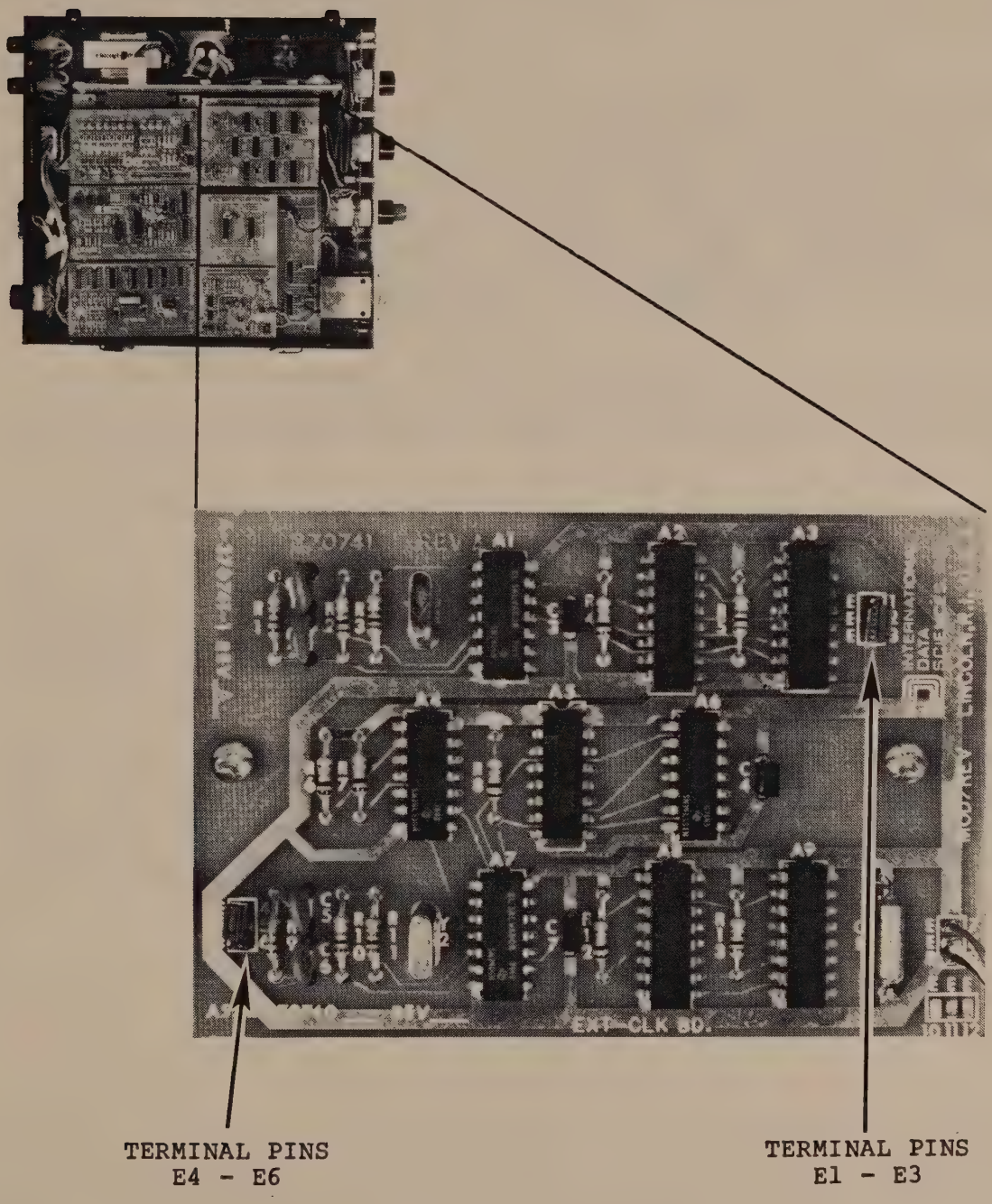


Figure 4-10. External Clock Strap Locations

4.12 Western Union Low Level Interface

4.12.1 Description

This option allows the test set to operate with the Western Union Low Level (W.U.L.L.) interface. A male 25-pin connector wired to a plug-in P.C. board provides this interface. The interface connector is installed on the optional rear panel assembly (replacing TTL) and is labeled W.U.L.L. Table 4-6 lists and describes the function of each pin assignment. The rear panel INTERFACE SELECT rotary switch is labeled W.U.L.L. in the blank space below the RS-422/423 selection. This switch configures the test set to operate through the selected interface.

A six-foot 15-conductor cable, terminated with a female 25-pin connector at one end and 15 fork lug connectors at the other end, is provided to interconnect the test set with the data interface.

4.12.2 Strapping

The W.U.L.L. interface P.C. board provides strapping to allow SCTE to be derived from the standard data rate selections or from the external clock option (if installed). These straps are accessible by removing the top cover of the test set. Strapping is accomplished by positioning jumper plugs over terminal pins J45-1 through J45-4 and J46-1 through J46-3 found on the P.C. board.

Positioning a jumper plug over J45-1 and J45-2, and over J46-1 and J46-2 disables the SCTE timing source. Positioning a jumper plug over J45-2 and J45-3, and over J46-1 and J46-2 configures SCTE to be derived from the standard data rate selections. Positioning a jumper plug over J45-3 and J45-4, and over J46-2 and J46-3 configures SCTE to be derived from the external clock option.

TABLE 4-6. W.U.L.L. INTERFACE DESCRIPTION

PIN #	MNEMONIC NAME	DIRECTION		FUNCTION
		TO DTE	TO DCE	
1	FG			FRAME GROUND
2	TD		→	TRANSMIT DATA
3	RD	←		RECEIVE DATA
4	-			NOT USED
5	-			NOT USED
6	-			NOT USED
7	SG			SIGNAL GROUND
8	-			NOT USED
9	-			NOT USED
10	-			NOT USED
11	-			NOT USED
12	-			NOT USED
13	-			NOT USED
14	-			NOT USED
15	SCT	←		SERIAL CLOCK TRANSMIT
16	-			NOT USED
17	SCR	←		SERIAL CLOCK RECEIVE
18	-			NOT USED
19	-			NOT USED
20	-			NOT USED
21	-			NOT USED
22	-			NOT USED
23	-			NOT USED
24	SCTE		→	SERIAL CLOCK XMIT EXTERNAL
25	-			NOT USED

4.12.3 Electrical Specifications

Data Rate -	200 Kbps, maximum.
Binary One, Mark, Off -	-6.2V + or - .5V (no load), -1.5V + or - .25V (150 ohm load).
Binary Zero, Space, On -	+6.2V + or - .5V (no load), +1.5V + or - .25V (150 ohm load).
Receiver Impedance (Z_{in}) -	150 ohm + or - 5%.
Driver Protection -	Output protected against short circuit to ground.
Receiver Protection -	+ or - 6V without damage.

APPENDIX

7 WELLINGTON ROAD, LINCOLN, RHODE ISLAND 02865
(401) 333-6200 TWX: 710-384-1911

BAUDOT TYPE A

b7 →	0	0	0	0
b6 →	0	0	0	0
b5 →	0	1	0	1
1st HEX DIGIT	0	1	2	3
2nd HEX DIGIT →				
b4 b3 b2 b1				
0 0 0 0 0	space	E	space	3
0 0 0 1 1	T	Z	5	ᴺ
0 0 1 0 2	C_R	D	C_R	$
0 0 1 1 3	O	B	9	?
0 1 0 0 4		S		B_L
0 1 0 1 5	H	Y	#	6
0 1 1 0 6	N	F	⁹	!
0 1 1 1 7	M	X	•	/
1 0 0 0 8	L_F	A	L_F	_
1 0 0 1 9	L	W	)	2
1 0 1 0 A	R	J	4	⁹
1 0 1 1 B	G	U_C	&	U_C
1 1 0 0 C	I	U	8	7
1 1 0 1 D	P	Q	⁰	1
1 1 1 0 E	C	K	:	(
1 1 1 1 F	V	L_C	;	L_C

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b8 →	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
b7 →	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
b6 →	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
b5 →	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1st HEX DIGIT	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
2nd HEX DIGIT →																
b4 b3 b2 b1																
0 0 0 0	0	NU	DL	DS	30		&	–	70	80	90	A0	B0	{	}	\	0
0 0 0 1	1	SH	D1	SS	31	41	51	/	71	a	j	~	B1	A	J	E1	1
0 0 1 0	2	SX	D2	FS	SY	42	52	62	72	b	k	s	B2	B	K	S	2
0 0 1 1	3	EX	D3	23	33	43	53	63	73	c	l	t	B3	C	L	T	3
0 1 0 0	4	PF	RE	BP	PN	44	54	64	74	d	m	u	B4	D	M	U	4
0 1 0 1	5	HT	NL	LF	RS	45	55	65	75	e	n	v	B5	E	N	V	5
0 1 1 0	6	LC	BS	EB	UC	46	56	66	76	f	o	w	B6	F	O	W	6
0 1 1 1	7	▨	IL	EC	ET	47	57	67	77	g	p	x	B7	G	P	X	7
1 0 0 0	8	GE	CN	28	38	48	58	68	78	h	q	y	B8	H	Q	Y	8
1 0 0 1	9	RF	EM	29	39	49	59	69	`	i	r	z	B9	I	R	Z	9
1 0 1 0	A	MM	CC	SM	3A	4A	!	6A	:	8A	9A	AA	BA	CA	DA	EA	FA
1 0 1 1	B	VT	C1	C2	C3	•	$	,	#	8B	9B	AB	BB	CB	DB	EB	FB
1 1 0 0	C	FF	IF	2C	D4	<	*	%	@	8C	9C	AC	BC	CC	DC	EC	FC
1 1 0 1	D	CR	GS	EQ	NK	(	)	_	'	8D	9D	[	]	CD	DD	ED	FD
1 1 1 0	E	SO	IR	AK	3E	+	;	>	=	8E	9E	AE	BE	CE	DE	EE	FE
1 1 1 1	F	SI	US	BL	SB	¦	^	?	"	8F	9F	AF	BF	CF	DF	EF	FF

EBCDIC CODE CHART

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(401) 333-6200 TWX: 710-384-1911

INTERNATIONAL DATA SCIENCES, INC.

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INTERNATIONAL DATA SCIENCES, INC.

	lower case								upper case							
b7 →	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
b6 →	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
b5 →	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1st HEX DIGIT	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2nd HEX DIGIT ↓ (b4 b3 b2 b1)																
0 0 0 0	0		8	@		_			h		*	4A		_			H
0 0 0 1	1					Y		q	&					Y		Q	+	
0 0 1 0	2	1				z		r	a		=			Z		R	A	
0 0 1 1	3	SPACE	9	/		j			i	SPACE	(	?		J			I	
0 1 0 0	4	2						b		<						B		
0 1 0 1	5		&	s		k					)	S		K				
0 1 1 0	6		#	t		l			•		"	T		L				^
0 1 1 1	7	3			,		$	c		;			,		!	C		
1 0 0 0	8	4			B_P		R_E	d		:			B_P		R_E	D		
1 0 0 1	9		P_N	u		m			P_F		P_N	U		M			P_F	
1 0 1 0	A		R_S	v		n			H_T		R_S	V		N			H_T	
1 0 1 1	B	5			L_F		N_L	e		%			L_F		N_L	E		
1 1 0 0	C		U_C	w		o			L_C		U_C	W		O			L_C	
1 1 0 1	D	6			E_B		B_S	f		,			E_B		B_S	F		
1 1 1 0	E	7			E_C		I_L	g		>			E_C		I_L	G		
1 1 1 1	F		E_T	x		p					E_T	X		P			▨	

2740/2741 EBCD CHART

PARS CODE CHART

b7 →				0	0	0	0
b6 →				0	0	1	1
b5 →				0	1	0	1
b8 = 0				1st DIGIT			
b4	b3	b2	b1	2nd DIGIT	0	1	2	3
0	0	0	0	0			▨	$
0	0	0	1	1	1	/	J	A
0	0	1	0	2	2	S	K	B
0	0	1	1	3	3	T	L	C
0	1	0	0	4	4	U	M	D
0	1	0	1	5	5	V	N	E
0	1	1	0	6	6	W	O	F
0	1	1	1	7	7	X	P	G
1	0	0	0	8	8	Y	Q	H
1	0	0	1	9	9	Z	R	I
1	0	1	0	A	↺	–	:	?
1	0	1	1	B	*	#	<	.
1	1	0	0	C	L_F		+	%
1	1	0	1	D	E_M	E_C	E_X	E_B
1	1	1	0	E	=	S_M	)	↕
1	1	1	1	F	@	,	(	S_Y

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S →	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
B →	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
A →	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
8 →	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
1st HEX DIGIT	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
2nd HEX DIGIT → (b4 b3 b2 b1)																
0 0 0 0	0		4	t		!			/		$	T					?
0 0 0 1	1					I		o	i					L		O	J	
0 0 1 0	2	1				h		s	g		[			H		S	G	
0 0 1 1	3					m			y			)	X		M			Y
0 1 0 0	4	2		x				=		@							+	
0 1 0 1	5		Z			•					Z	N			•			
0 1 1 0	6		9	n		v			—		(	U			V			^
0 1 1 1	7	3		u		b		w	f		#			B		W	F	
1 0 0 0	8	5				B_P		R_E	p		%			B_P		R_E	P	
1 0 0 1	9		P_N			,			P_F			P_N	E		H			P_F
1 0 1 0	A		R_S	e		r			H_T			R_S	D		R			H_T
1 0 1 1	B	7		d		L_F		N_L	;		&			L_F		N_L	:	
1 1 0 0	C		U_C			i			L_C			U_C	K		I			L_C
1 1 0 1	D	6		k		E_B		B_S	q		4A			E_B		B_S	Q	
1 1 1 0	E	8				E_C		I_L	,		*			E_C		I_L	,	
1 1 1 1	F		E_T	c		a						E_T	C		A			

SELECTRIC CODE CHART

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INTERNATIONAL DATA SCIENCES, INC.

SIX-BIT TRANSCODE CHART

2nd DIGIT \ 1st DIGIT	0	1	2	3
0	S_H	&	-	ø
1	A	J	/	1
2	B	K	S	2
3	C	L	T	3
4	D	M	U	4
5	E	N	V	5
6	F	O	W	6
7	G	P	X	7
8	H	Q	Y	8
9	I	R	Z	9
A	S_X		E_C	S_Y
B	•	$	,	#
C	<	*	%	@
D	B_L	U_S	E_Q	N_K
E	S_B	E_T	E_X	E_M
F	E_B	D_L	H_T	▨

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UNIVAC FIELD DATA
AFTER 1-8 REVERSAL

0 →	0	0	0	0
0 →	0	0	0	0
b6 →	0	0	1	1
b5 →	0	1	0	1
1st HEX DIGIT	0	1	2	3
2nd HEX DIGIT →				
b4 b3 b2 b1				
0 0 0 0 0	@	]	[	#
0 0 0 1 1	)	+	–	<
0 0 1 0 2	K	M	L	N
0 0 1 1 3	↺	2	1	3
0 1 0 0 4	C	E	D	F
0 1 0 1 5	*	%	(	:
0 1 1 0 6	S	U	T	V
0 1 1 1 7	8	'	9	;
1 0 0 0 8	∧	A	space	B
1 0 0 1 9	=	&	>	$
1 0 1 0 A	O	Q	P	R
1 0 1 1 B	4	6	5	7
1 1 0 0 C	G	I	H	J
1 1 0 1 D	?	,	!	/
1 1 1 0 E	W	Y	X	Z
1 1 1 1 F	/	▨	•	¡

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MODEL 1320 SPARE PARTS LIST

QTY.	PART NO.	REF. DESIG.	DESCRIPTION	VENDOR	REMARKS
1	7-370410	A1 Board	P.C. Bd. Assembly	IDS	
1	7-370420	A2 Board	P.C. Bd. Assembly	IDS	
1	7-370430	A3 Board	P.C. Bd. Assembly	IDS	
1	7-370440	A4 Board	P.C. Bd. Assembly	IDS	
1	7-370488	AC Ass'y	Power Switch Sub Ass'y	IDS	
1	7-400000-1	CBL Ass'y	EIA Data Cable	IDS	
2	6-360-8	73	Knob	IDS	
1	6-360-6	74	Knob	IDS	
1	6-360-11	75	Knob	IDS	
1	6-501-110120	M1	Meter	IDS	
1	6-452-1104	S1	Rotary Switch	IDS	
1	6-452-1102	S2	Rotary Switch	IDS	
1	6-452-1107	S3	Rotary Switch	IDS	
1	6-290-11	F1	1 Amp SB Fuse	IDS	
1	6-290-3	F2	½ Amp SB Fuse	IDS	
1	6-432-600001	P1	A.C. Line Cord	IDS	

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CALIBRATION AND REPAIR SERVICE

All units sold by International Data Sciences, Inc. are calibrated at the time of delivery. International Data Sciences, Inc. recommends a periodic calibration every six months thereafter performed by the Calibration Department at International Data Sciences, Inc. Contact IDS for the cost of each calibration. If the unit requires repairs not covered by the original warranty, then IDS will perform the repair at an hourly charge plus parts. Normal turnaround time for calibration or repair is two weeks.

Equipment so calibrated will bear a gummed label on the rear panel identifying the serial number of unit calibrated, the date of calibration, the next recommended calibration date, and the in-plant calibrator identifier.

Prior to shipping your unit, contact IDS at (401) 333-6200 for a Return Authorization Number (RMA) number. This is required for all units returned for calibration or repair.

All units returned to IDS for calibration or repair will be accepted only if transportation charges are prepaid. The purchaser is also responsible for all transportation charges incurred in returning the calibrated unit to the purchaser.

For fast returns, Federal Express or Emery Air Freight are recommended; otherwise, units will be returned via UPS. Return address should be clearly stated and should include a person to the attention of whom unit will be shipped.

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INTERNATIONAL DATA SCIENCES, INC.

MODEL 1320 TROUBLE REPORT

1) Please indicate what positions the following switches were in:

PATTERN	CODE LEVEL	BLOCK SIZE	DATA RATE	
___ 2047	___	___ 10^3	___ 9600	___ 300
___ 511	___ 8	___ 10^4	___ 4800	___ 150
___ 63	___ 7	___ 10^5	___ 1800	___ 134.5
___ ALT	___ 6	___ 10^6	___ 1200	___ 110
___ MARK	___ 5	___ 10^7	___ 600	___ 75
___ SPACE		___ 10^8		___ EXT

STOP BITS	INV. DATA/NORM	PARITY	START TEST
___ 1	___ INV. DATA	___ EVEN	___ SINGLE
___ 1.4	___ NORM	___ NO	___ CONT.
___ 2		___ ODD	

BLOCK/BIT ERROR	ASYNC/SYNC	-3/NORM
___ BLK/CHR ERR	___ ASYNC	___ -3
___ BIT ERR	___ SYNC	___ NORM

SELF TEST/OPERATE	DATA/PATTERN	SINGLE/CONT
___ SELF TEST	___ DATA	___ SINGLE
___ OPERATE	___ PATTERN	___ CONT

RTS/CTS	DTR/CTS	BUSY/RI	INTERFACE SELECT	
___ RTS/CTS	___ DTR/CTS	___ BUSY/RI	___ RS-232	___ 303
___ OFF	___ OFF	___ OFF	___ TTL	___ MIL-188
			___ V.35	___ TTY
			___ RS-422	

2) Please draw or give a description of how the test set was being used. Describe interface used, equipment type, and malfunction. (Attach additional sheets if necessary.)

3) Give name, address, and telephone number of person to contact about this unit.

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WARRANTY

All International Data Sciences, Inc. products are warranted against defects in material, workmanship, and component failure for one year unless noted otherwise. All units repaired by IDS are warranted for 90 days following the repair service.

All units returned to IDS under this warranty require prepaid transportation charges. The purchaser is also responsible for all transportation charges incurred in returning the repaired unit to the purchaser.

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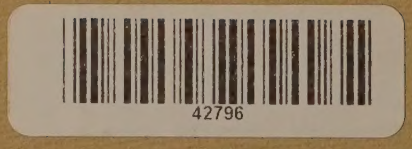

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